AF
27 02
34
8-13-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	**TIF-15767A**
Gerard Chauvel, et al.	Examiner: **Tran, D.**
Serial No.: **08/890,894**	Art Unit: **2186**
Filed: **07/10/97**	Conf. No.: **5253**

For: **MULTIPLE PROCESSOR APPARATUS HAVING A PROTOCOL PROCESSOR INTENDED FOR THE EXECUTION OF A COLLECTION OF INSTRUCTIONS IN A REDUCED NUMBER OF OPERATIONS**

RECEIVED

REPLY BRIEF

AUG 0 7 2003

Technology Center 2100

Commissioner for Patents

Alexandria, VA 22313-1450

Dear Sir:

In support of their appeal of the Final Rejection of claims in the above-referenced application, and in response to the Examiner's Answer dated June 3, 2003, Appellants respectfully submit herein their Reply Brief.

APPELLANTS' RESPONSE

1) <u>Reply to Examiner's Response #1 (page 15, lines 5-11)</u>.

The Examiner argues:

In response to appellant's argument that the references fail to show certain features of appellant's invention, **it is noted that the feature upon which appellant relies (i.e., program memory in the B processor or none of the memory was within the B processor) are not recited in the rejected claim(s).** Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims.

Appellants reaffirm their previous arguments. Additionally, Appellants respectfully respond that that there is no basis whatsoever for the Examiner's above nonsensical argument. Each of the relevant claims requires that each of its processors has a "program memory". As such, each processor must have a "program memory". Finch's Fig. 1 clearly shows that processor "B" does not comprise a "program memory" or any other memory for that matter. Whether or not the claims state "in", the fact remains that each of the processors of the claims MUST have a "program memory" – whether or not "in" is in the claims. The facts clearly show that there is NO "program memory" IN or WITHIN or REQUIRED BY or PART OF Finch's processor B. As a result, the Examiner's argument is without merit.

2) Reply to Examiner's Response #1 (page 15, lines 14-22).

The Examiner argues:

The examiner disagrees with the appellant's arguments because Finch teaches the B processor **comprising** a program memory (fig. 1, common memory RAM, local "B" and col. 8, lines 37-41) **as recited in the claims 36-39.** Even though, the common memory, RAM local to "B" is not within the B processor physically, it is still the program memory of the B processor because it is accessible to the B processor and it stores software for execution of the B processor and it is the memory of the B processor, then it is a part (i.e., comprising) of the B processor and it is in B logically.

Appellants reaffirm their previous arguments. Additionally, Appellants respectfully respond that the Examiner admits that the common memory, RAM local to "B" is not within Finch's B processor (page 15, lines 17-18). Indeed, Finch clearly shows in Fig. 1 that "RAM local to "B", while coupled to "B" processor, is NOT part of "B processor".

Nevertheless, the Examiner attempts to distort the argument by stating that the "common memory" is logically part of "B" processor. Using the Examiner's logic, there really is no "A" processor and "B" processor – there is just one bit conglomeration since each of the processors are "logically" part of each other. Appellants respectfully point out that the language of each of Claims 36-39 requires that each of its processors "comprise" a "program memory". Finch's Fig. 1 clearly shows that "B" processor does not comprise a "program memory", as required by Claims 36-39.

Appellants respectfully submit that in order for the rejection of Claims 36-39 be sustainable, it is fundamental that "each and every element as set forth in the claims be found, either expressly or inherently described, in a single prior art reference." Verdegall Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim". Appellants have clearly shown above that "each and every element as set forth in Claims 36-39 are NOT found, either expressly or inherently described, in the Finch reference. Accordingly, the 35 U.S.C. 102(a) rejection of Claims 36-39 over Finch should be reversed.

3) Reply to Examiner's Response #2 (page 16, line 1 – page 17, line 5).

Appellants reaffirm their arguments set forth in the Appeal Brief (page 14, line 24 – page 15, line 14).

4) Reply to Examiner's Response #3 (page 17, lines 12-17).

The Examiner's motivation:

As to point (3) even though Asano teaches vector processors and Aoyama teaches a vector processor and a scalar processor, both of the references teach controlling a plurality of processors for accessing a common memory. Therefore, the examiner would apply the teaching of each processor comprising ROM, a RAM (e.g., Asano, fig. 1, els 22-23) and one and only one common memory (e.g., Asano, fig. 17 and 6, els 62, 172 and fig. 1, el. 14a coupling the processors to a common memory 1).

Appellants reaffirm their previous arguments. Additionally, Appellants respectfully respond point out that this argument is not consistent with the Examiner's previous determination where the Examiner admitted Aoyama, "does not show the use each of the processors comprising a local memory and a program memory **and one and only one common memory** (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor" (Office Action dated June 6, 2002, page 3, line 18 – page 4, line 1). The Examiner relies upon Asano as "teaching the concept and advantages of each processor having a local memory and a program memory **and a common memory** for coupling the local memory of a first processor to the local memory of a second memory" (Office Action dated June 6, 2002, page 4, lines 1-4) – NOT on both Aoyama and Asano teaching this same concept. Moreover, the Examiner has not explained this apparent change in reasoning or support in the references for such change.

5) Reply to Examiner's Response #3 (page 17, line 21 – page 18, line 6).

The Examiner set forth the following motivation for combining Asano and Aoyama (page 17, line 21 – page 18, line 7):

It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama **because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor.**

Appellants reaffirm their previous arguments. Additionally, Appellants respectfully respond that the Examiner's above determination is supposition not supported by fact. The Examiner has provided no evidence whatsoever that the Examiner's purported modification of Aoyama will result increased processing speed of each processor. Where is the evidence that such modification will produce such results? Even the Examiner admits that he cannot combine the two references. Simply put, the Examiner has not established a prima facie case of the obviousness.

Moreover, Appellants respectfully submit that the Examiner's purported combination of Asano and Aoyama is improper. More particularly, Appellants traverse the Examiner's interpretation of Asano and point out that Asano's processor DMM1-DMMk (11a-11k) are ALL digital signal processors (Figs. 1 & 2; Col. 9, lines 46-53) which are used exclusively for video signal processing (col. 5, lines 50-55; col. 6. lines 57- col. 8. line 21). Accordingly, since each unit processor DMM1-DMMk is in charge of processing image signals for a plurality of sectional frames which are not contiguous but separated from each other, and all the unit processor simultaneously begin processing in synchronism with the state of a new picture frame, each of processors DMM1-DMMk appear to perform "vector" processing, and not "scalar" processing. Accordingly, it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing, without the improper hindsight provided by Appellants' disclosure.

6) Reply to Examiner's Response #3 (page 18, lines 7-11).

The Examiner argued:

In further discussion, the examiner would **apply the teaching of Asano** as discussed above to modify the Aoyama **but would not physically combine the two systems together**. Basically, the feature is very well known in any

type of computer architecture field. The examiner is simply choosing one of many to use as an example, to show Appellants' claimed features.

Appellants reaffirm their previous arguments. Additionally, Appellants respectfully traverses the Examiner determination. More particularly, the Examiner never addresses the distinction between Aoyama (which discloses one vector processor and one protocol processor) and Asano, which discloses two vector processors. The Examiner had previously argued that the teachings of one can be lumped into the teaching of the other. Now, the Examiner states that "he would apply the teaching of Asano as set forth by the Examiner to modify the Aoyama but would not physically combine the two system together (Office Action dated June 6, 2002). Obviously, the reason why the Examiner will not combine the two references is because they CANNOT be combined! The Examiner provides no teaching from the prior art that indicates that the teaching of Asano can be combined with Aoyama in order to modify Aoyama, with any hope of success in arriving at a modified apparatus that obviates the present invention. Where is the evidence that such a combination is possible or even contemplated? The Examiner's determination is supposition not supported by fact.

7) <u>Reply to Examiner's Response #4 (page 18, line 20 – page 19, line 6)</u>.

The Examiner argued:

Even though the examiner used Aoyama to show the use of the synchronizing circuit (e.g., fig. 1, els. 810 or 800a, col. 5, lines 1-10), also, Asano clearly teaches or suggests a synchronizing circuit for coupling the core of the first processor to the core of said second processor (e.g., col. 10, lines 15-30; fig. 6, el. 71 controlling the plurality processors to access a common memory 62; and col. 12, lines 58-61;). It does not matter whether Asano teaches or does not teaches a synchronizing circuit for coupling the core of said first processor to the core of said second processor because Aoyama teaches the feature as stated in the rejection above.

Appellants reaffirm their previous arguments. Additionally, Appellants respectfully respond that it does in fact matter whether or not Asano teaches a synchronizing

circuit for coupling the core. If, as suggested by Appellants, Asano does not provide such teaching, failure to do so could directly impact any decision by one having ordinary skill in the art to combine Asano's teaching with Aoyama's. And, as previously stated, Asano fails to teach or suggest a "synchronizing circuit for coupling said core of said first processor to said core of said second processor", as required by Claims 6 and 36. This is yet another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

8) <u>Reply to Examiner's Response #5 (page 20, line 4 – page 21, line 13)</u>.

The Examiner argued (page 20, lines 4-9):

Asano clearly discloses one and only one common memory coupling said first processor to said second processor," as recited in the claim 36 (e.g., fig. 6, a common memory 62; and col. 12, lines 53-61; fig. 1, el. 14a coupling the processors to a common memory 1, or figs. 6 and 17, els. 62, one and only one common memory 172 coupled to processor 173a-173b and local memories 174a-174b).

Appellants reaffirm their previous arguments. Additionally, Appellants respectfully respond that Asano fails to teach or suggest, "one and only one common memory coupling the first processor to the second processor", as required by Claim 36. While Asano's Fig. 6 shows DSP 63a, 63b ...63n, coupled to each other and to common memory 62, memory 62 does NOT couple any one of DSPs 63a-63n. Similarly, Fig. 1 fails to show any one of common memories 10a-10n coupling any one of processors 11a-11k to another one of processors 11a-11k.

The Examiner further argued (page 20, line 1 – page 21, line 2):

Furthermore, Asano, fig. 1 and col. 12, lines 3-15, shows at some specific time, only the modules processor 11a and 11b request access to the common memories, one and only one common memory 1 or 10a couples the processor module 11a to processor module 11b while the other memory buses are idle. Therefore, Asano, fig. 1, shows "one and only one common memory coupling the first processor to the second processor".

Appellants reaffirm their previous arguments. Additionally, Appellants respectfully respond that Asano discloses "multiple" common memories coupled to multiple processors – NOT coupling any one processor to another since all of the processors are already coupled to each other. The fact remains that all of the processors in Asano are coupled to all of the common memories in Asano. This is yet another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

9) Reply to Examiner's Response #6 (page 21, line 4 – page 21, line 13).

The Examiner argued (page 21, line 20 – page 22, line 14):

Asano teaches many different ways for coupling the local memory of the first processor to the local memory of the second processor (e.g., fig. 17, coupling by only memory bus or coupling by the common memory 172 and memory bus). Fig. 17, Asano shows a common memory 172 and the bus 176 coupling a local memory 174a of processor 1 to a local memory 174b of processor 2. In particular, fig. 17, Asano shows coupling data from the local memory 174a of the first processor to the common memory (e.g., col. 2, lines 15-20) and coupling data from the common memory to the local memory 174b of the second processor (e.g., col. 2, lines 5-10).

Appellants reaffirm their arguments on page 18, lines 1-12 of Appellants' Brief. Furthermore, Appellants respectfully respond that the Examiner is NOT considering all of the words of the claim and is instead reading words into the claims that are not there. Independent Claim 6 requires and positively recites, "a memory circuit **for coupling said**

local memory of said first processor to said local memory of said second processor". Independent Claim 36 requires and positively recites, **"one and only one common memory coupling said local memory of said first processor to said local memory of said second processor".** The claims say nothing whatsoever about "coupling data", as argued by the Examiner. Further, local memories 174a-17h of Asano are coupled to each other regardless of frame store/common memory 172 (see Fig. 17). The same can be said for the teaching of Fig. 1. As a result, the argument of the Examiner is supposition not supported by fact.

10) Reply to Examiner's Response #7 (page 22, line 15 – page 23, line 7).

Appellants reaffirm their previous arguments that Shimoda does not teach what is proposed by the Examiner (Appeal Brief, page 18, lines 13-19). Moreover, even if, arguendo, Shimoda teaches, "the S-unit access to storage 5A (5B), **and when the data is not present, the S-unit 3a (3b) directly accesses to the common memory 7c ...",** as suggested by the Examiner, the teaching of Shimoda supports the Appellants position by teaching that when data is not present, **"when the data is not present, the S-unit 3a (3B) directly accesses to the common memory 7c",** which means Shimoda does not teach or suggest, "the use of having data from a local cache 3A instead of having data from a common memory 7c **every time** to increase processing speed". As a result, Shimoda does not support the Examiner's argument.

11) Reply to Examiner's Response #8 (page 22, line 15 – page 23, line 7).

Appellants reaffirm their previous arguments that Shimoda and Morris Mano fail to provide any additional teaching that "it would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one memory for coupling the

local memory of a first processor to the local memory of a second memory into the system of Aoyama **because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor**", as suggested by the Examiner. The Examiner's determination is nothing more than improper hindsight reconstruction. The Examiner has also cited no art that suggests that Asano's accessing speed of its main memory is a problem that needs correcting.

12) Reply to Examiner's Response #9 (page 24, line 4 – page 25, line 5).

Appellants reaffirm their previous arguments. Additionally, Appellants again traverse the Examiner's determination that "it does not matter whether Asano teaches or does not teaches a synchronizing circuit for coupling the core of said first processor to the core of said second process because Aoyama teaches the feature as stated in the rejection above" (Examiner's Answer, page 24, lines 17-19; Office Action dated June 6, 2002, page 16, lines 8-11). Appellants respond that it certainly does matter! It goes to the core of whether or not one of ordinary skill in the art at the time of the invention would have been motivated to combine the two teachings. The Examiner cannot simply "pick and choose" amongst the prior art disclosure in order to selectively obviate the present invention – the Examiner must show evidence in the prior art for such motivation.

13) Reply to Examiner's Response #10 (page 25, lines 6-12).

Appellants reaffirm their previous arguments. No additional argument is necessary.

14) Reply to Examiner's Response #11(page 25, line 13 – page 26, line 17).

Appellants reaffirm their previous arguments. No additional argument is necessary.

15) Reply to Examiner's Response #12 (page 27, lines 1-7).

Appellants reaffirm their previous arguments. Moreover, there is no merit to the Examiner's argument is arguing limitations not supported by the claims. Appellants previously argued that Aoyama fails to teach or suggest a "main processor" as required by the claims (Appeal Brief, page 23, lines 4-13). Reference to DMM1-DMMk was made solely with regard to Aoyama whose processors are identified as DMM1-DMMk, none of which was identified as being a "main processor". As a result, the Examiner's argument is without merit.

16) Reply to Examiner's Response #12 (page 27, lines 8-13).

Appellants reaffirm their previous arguments. Moreover, there is no merit to the Examiner's argument that Aoyama teaches that the second processor is the main processor of the system. It is the Examiner, and not Aoyama, that proposes that Aoyama's vector processor is the main processor of the system. Once again, this is hindsight reconstruction on the part of the Examiner.

17) Reply to Examiner's Response #13 (page 27, line 14 -7).

Appellants reaffirm their previous arguments. No additional argument is necessary.

18) Reply to Examiner's Response #14 (page 28, lines 1 – 17).

Appellants reaffirm their previous arguments. No additional argument is necessary.

19) Reply to Examiner's Response #15 (page 28, line 17 – page 29, line 5).

Appellants reaffirm their previous arguments. No additional argument is necessary.

20) Reply to Examiner's Response #16 (page 29, line 10 – page 30, line 5).

Appellants reaffirm their previous arguments. No additional argument is necessary.

21) Reply to Examiner's Response #17 (page 30, line 6 – page 31, line 5).

Appellants reaffirm their previous arguments. Moreover, the examiner basis his whole "obviousness" argument on the following: if something increases processing speed of each processor – it must be obvious since it is desirable. Using the Examiner's argument, every invention that increases processing speed would be obvious since it is desirable. Where is proof from the prior art that supports the Examiner's statement?

22) Reply to Examiner's Response #18 (page 31, line 16 – page 32, line 15).

Appellants reaffirm their previous arguments. Moreover, the examiner basis his whole "obviousness" argument on the following: if something increases processing speed of each processor (by having local memories and program memories instead of a main storage) – it must be obvious since it is desirable to increase processing efficiency for each processor. Using the Examiner's argument, every invention that increases processing speed would be obvious since it is desirable. Where is proof from the prior art that supports the Examiner's statement?

23) Reply to Examiner's Response #19 (page 32, line 16 – page 34, line 8).

Appellants reaffirm their previous arguments. Moreover, the examiner basis his whole "obviousness" argument on the following: if something increases processing speed of each processor – it must be obvious since it is desirable. Using the Examiner's argument, every invention that increases processing speed would be obvious since it is desirable. Where is proof from the prior art that supports the Examiner's statement?

24) Reply to Examiner's Response #20 (page 33, line 1 – page 34, line 8).

Appellants reaffirm their previous arguments. Moreover, the examiner basis his whole "obviousness" argument on the following: if something increases processing speed of each processor – it must be obvious since it is desirable. Using the Examiner's argument, every invention that increases processing speed would be obvious since it is desirable. Where is proof from the prior art that supports the Examiner's statement?

25) Reply to Examiner's Response #21 (page 34, lines 9-14).

Appellants reaffirm their previous arguments. No additional argument is needed.

26) Reply to Examiner's Response #22 (page 34, line 15 – page 35, line 12).

Appellants reaffirm their previous arguments. Moreover, the examiner basis his whole "obviousness" argument on the following: "it would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing into Aoyama because **it would allow protocol processing to be performed, thereby, increasing system computation power and functionality**". Using the Examiner's argument, every invention that "allows protocol processing to be perform" that "increases system computation power and functionality", would be obvious since it is desirable. Where, however, is proof from the prior art that supports the Examiner's statement? Once again, the Examiner's determination is hindsight reconstruction.

27) Reply to Examiner's Response #23 (page 35, line 13 – page 36, line 20).

Appellants reaffirm their previous arguments. Moreover, the examiner basis his whole "obviousness" argument on the following: if something provides signal processing capability to suit a special purpose application – it increases system functionality which must be obvious since it is desirable. Using the Examiner's argument, every invention that increases system functionality would be obvious since it is desirable. Where is proof from the prior art that supports the Examiner's statement?

28) Reply to Examiner's Response #24 (page 37, lines 1–20).

Appellants reaffirm their previous arguments. Moreover, the examiner basis his whole "obviousness" argument on the following: if something allows protocol processing to be performed and parallel computations on large arrays to be performed, thereby, increasing system computation power and functionality – it must be obvious since it is desirable. Using the Examiner's argument, every invention that allows protocol processing to be performed and parallel computations on large arrays to be performed, thereby, increasing system computation power and functionality would be obvious since it is desirable. Where is proof from the prior art that supports the Examiner's statement?

29) Reply to Examiner's Response #25 (page 38, line 1 – page 39, line 7).

Appellants reaffirm their previous arguments. No additional argument is needed.

30) Reply to Examiner's Response #26 (page 39, line 1 – page 40, line 2).
Appellants reaffirm their previous arguments. No additional argument is needed.

31) Reply to Examiner's Response #27 (page 40, lines 3–11).

Appellants reaffirm their previous arguments. No additional argument is needed.

32) Reply to Examiner's Response #28 (page 40 lines 12–16).

Appellants reaffirm their previous arguments. No additional argument is needed.

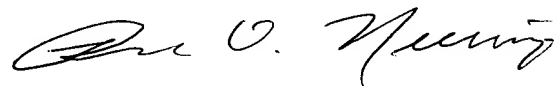33) Reply to Examiner's Response #29 (page 40, line 17 – page 41, line 13).

Appellants reaffirm their previous arguments. Moreover, the examiner basis his whole "obviousness" argument on the following: if something could be used to perform protocol processing in Aoyama, it would be obvious since it would "allow protocol processing to be performed" – it must be obvious since it is desirable. Using the Examiner's argument, every invention that could be used to allow Aoyama to perform "protocol processing" – would be obvious since it is desirable.

34) Reply to Examiner's Response #30 (page 41, lines 14–19).

Appellants reaffirm their previous arguments. No additional argument is needed.

For the above reasons, favorable consideration of the appeal of the Final Rejection in the above-referenced application, and its reversal, are respectfully requested.

Respectfully submitted,

Ronald O. Neerings
Reg. No. 34,227
Attorney for Appellants

TEXAS INSTRUMENTS INCORPORATED
P.O. BOX 655474, M/S 3999
Dallas, Texas 75265
Phone: 972/917-5299
Fax: 972/917-4418